Analogy Competition

I Main Concepts:

- **A Organization**
- **B Amdahl's Law - Cost/Perf.**
- **C RISC vs. CISC**
- **D Transistors**
- **E Single Cycle vs. Multicycle**
- **F Pipeline**
- **G Hazards**
- **H Interrupts**
- **I Microprogramming**

Analogy Competition

I Main Concepts:

- **J Memory Hierarchy**
- **K Cache**
- **L DRAM and SRAM**
- **M Virtual Memory**
- **N Bus Interface**
- **O DMA**
- **P Input and Output**
- **Q Networks (LAN/WAN)**
- **R Massively Parallel Processors**

Administrative

I Extra Credit

II Final Presentation Due 4/26

III Final Report Due 5/3

Final Project Write-up

I Format is On-line +

II Extension of Labs Subjects Suggestions:

- **A Super-scalar (PowerPC like)**
- **B Super-pipeline (Alpha like)**
- **C VLIW RISC Processor**
- **D MPPs**
- **E Coprocessors (Math Copr.)**
- **F Optimization (4way cache, min-cyc)**

Caches and PCI

I Question

II PCI Interface

III What problems?

IV Solutions

V Real Issues

Interconnection

I Datapath

II Bus

III Networks

CS 152

Discussion Section 102: Friday 12:30-2

Discussion Note #13: April 19, 1996

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Agenda

I Caches and PCI done

II Interconnecttion

III Administrative/Break (5 min)

IV Final Project Write-up

V Analogy Competition/Ex.Cr.

VI Lab 6 Write up due