

CS152
Computer Architecture and Engineering
Discussion Section 102: Disc #2
ISA and Gates

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Young H. Cho (youngc@cory)
Slides available on <http://www.csua.berkeley.edu/~young>

Overview of Today's Discussion: ISA and Gate Technology

- ♣ Review from Last Discussion (20 min)
- ♣ ISA (20 min)
- ♣ Break (3 min)
- ♣ Administrative (5 - 10 min)
- ♣ Gate Technology (20 min)
- ♣ Break (3 min)
- ♣ HW Questions (...)

Review from Last Discussion

- A. Computer = Control, Datapath / Memory / Input, Output
 - Interconnections = BUS (MBus, Mem Bus, SCSI, Ext Bus)
- B. Memory Hierarchy - Registers -> Cache -> Main Mem -> Disk...
- C. IC Costs
- D. Performance = inverse Execution Time
- E. CPU Performance (CPI, MIPS, MFLOPS, Amdahl's Law)
- F. RISC versus CISC

Cost of Dies

Cost of die = Cost of wafer / (Dies per wafer X Die yield)

Dies per wafer = $\frac{\pi \times (\text{Wafer diam}/2)^2}{\text{Die Area}}$ - Test die
 $\frac{\pi \times \text{Wafer diam}}{\text{sqrt}(2 * \text{Die A})}$

Die yield = Wafer yield X $\{ 1 + \frac{\text{Defects per unit area} \times \text{Die area}}{\alpha} \}^{-\alpha}$

$\alpha = 2.0$ for simple MOS process and higher for BiCMOS

* ex. wafer yield 90%, defct/unit = 2/cm², die area = 1 cm²
then die yield ~ 22.5%

Performance

Performance = 1 / Execution Time

$$\text{CPI} = \sum_{i=1}^n \text{cpi}_i \times \text{freq}_i ; \quad \text{freq} = \frac{I}{\text{Instruction Count}}$$

$$\text{MIPS} = \text{Instruction Count} / (\text{Time} \times 10^6) = \text{Clock rate} / (\text{CPI} \times 10^6)$$

$$\text{MFLOPS} = \text{FP op} / (\text{Time} \times 10^6)$$

Benchmarks

SPEC - System Performance Evaluation Cooperative

$$\text{CPU time} = (\text{Instr} / \text{Prog}) \times (\text{Cycles} / \text{Instr}) \times (\text{Sec} / \text{Cycle})$$

$$\text{Amdahl's Law} \rightarrow \text{Speedup}(w/E) = \frac{\text{ExTime}(w/o E)}{((1-F)+F/S) \times \text{ExTime}(w/o E)}$$

Instruction Set Architecture

Stack:

operands on top of stack

Accumulator:

one operand is implicitly the accumulator

General Purpose Register:

Register/Memory:

only explicit operands - either memory or registers
access memory as part of any instruction

Load/Store:

access memory only with load/store

ISA Exercise

convert following to four different ISA assembly code:

A=B+C-D;

Accumulator

load addrB
add addrC
sub addrD
store addrA

Memory-to-Memory

add addrA, addrB, addrC
sub addrA, addrA, addrD

Stack

push D
push B
push C
add
sub
pop A

MIPS (Load/Store)

lw R1, addrB
lw R2, addrC
lw R3, addrD
add R4, R1, R2
sub R4, R4, R3
sw R4, addrA

Addressing modes

Data Addressing modes

42% Average - Displacement: Add R4, 100(R1)

33% Average - Immediate: Add R4, 3

13% Average - Register Indirect: Add R4, (R1)

Addressing Objects

Little endian - 7 6 5 4 word (Intel 80x86, DEC Vax, ...)

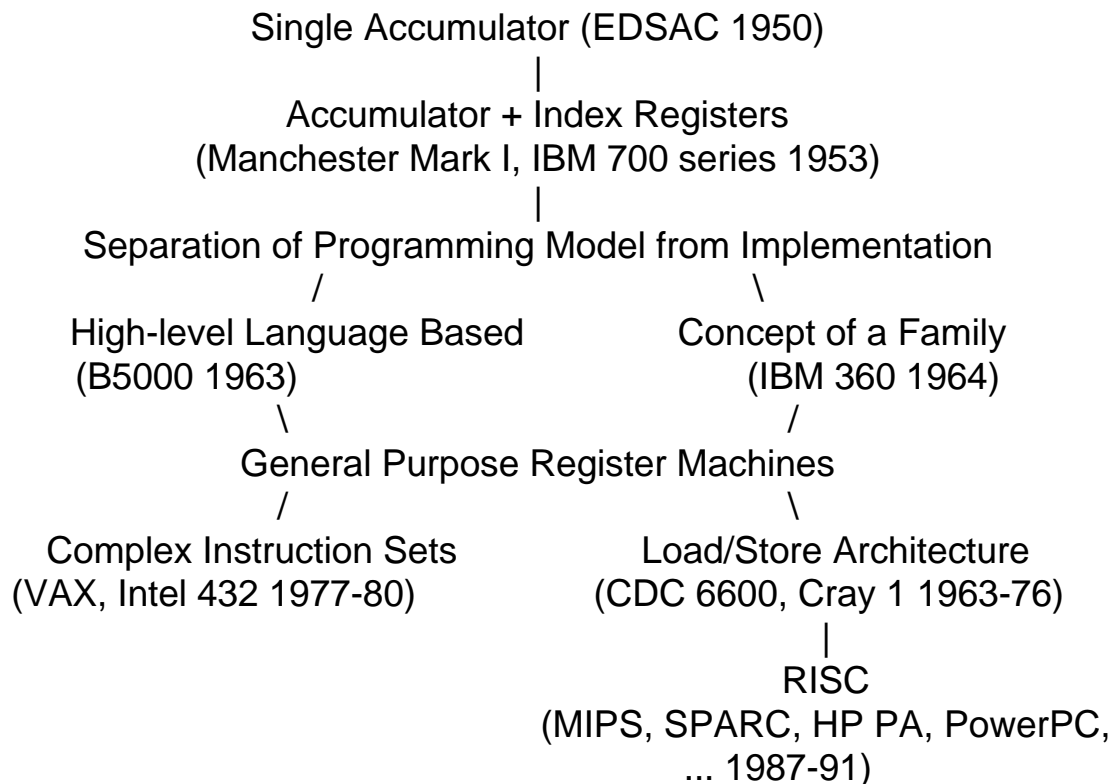
□□□□

Big endian - 0 1 2 3 word (MIPS, Motorola, HP PA, ...)

Operation:

Load 22%,
Store 12%,
Add 8%,
Subtract 5%,
Move reg-reg 4%,
And 6%,
Compare equal 16%,
Branch 20%,
Call 1%,
Return 1%

Total ~ 96%



80x86 v. DLX(RISC) Instruction Counts

<u>SPEC Program</u>	<u>x86</u>	<u>DLX</u>	<u>DLX/x86 Rt</u>
gcc	3,771,327,742	3,892,063,460	1.03
espresso	2,216,423,413	2,801,294,286	1.26
spice	15,257,026,309	16,965,928,788	1.11
nasa7	15,603,040,963	6,118,740,321	0.39

Pipeline

- Laundry Example
- Evident Speedup
- Hazards occur
- Patch things up - compiler tricks and hardware tricks

Hazards

1. Structural Hazard (IF and Mem stage both trying to use memory at the same time) - Any hazards caused by hardware
2. Data Hazard (Using register that is being calculated before the result has been stored into the register) - can be fixed up to a certain point by using forwarding unit
3. Control Hazard (Control hazards - usually caused by branch)

Delayed Branches - Redefined behavior

-By the end of the read stage of the Branch Instruction, the CPU knows whether or not the branch will take place. However, it will have fetched the next instruction by then, regardless of whether or not a branch will be taken.

-Compiler can fill a single delay slot with a useful Instruction 50% of the time.

Administrative

- Get names of students in Discussion
- Pair-up people for Assignment #2
- Midterm on Feb 22, 1995 Wednesday at 5pm-8pm at Sibley Auditorium
- Pizza at La Val's after Midterm (bring \$5.00)
- Homework #2, a lot of little programs
- Start making groups of 4 to 5
- Everyone in the team has to be in same discussion section
- No auditors may be in the team
- Office Hours: Young - Friday 2:30-3:30pm Soda 283
Oza - Thursday 4-5pm Soda 283

Basic Technology: CMOS

NMOS - Turns on when High (V_{dd} , 5V) is applied
(Analogy: Opens the gate at the hill to let the water flow
Gate controlled by stream of water - Water applied to
gate control opens the gate.)

Turns off when Low (Gnd, 0V) is applied

PMOS - Turns off when High (V_{dd} , 5V) is applied
(Analogy: Closes the gate at the hill to let the water flow
Gate controlled by stream of water - Water applied to
gate control opens the gate.)

Turns on when Low (Gnd, 0V) is applied

Gate Comparison

If PMOS transistor is faster: NOR gate is preferred

NMOS in Series

PMOS in Parallel

H to L is more critical than L to H

If NMOS transistor is faster: NAND gate is preferred

NMOS in Parallel

PMOS in Series

L to H is more critical than H to L

Internal Delay

Internal Delay of Circuit

= Sum of Internal Delay of Gates
+ (Wire Capacitance between two gates [i.e. Gate 1 and 2]
+ Gate 2 Input Capacitance)
x Load Dependant Delay of Gate 1

For Example:

Total Internal Delay from Input of G.1(A) to G.2(B) output
= I.D G1 + (Wire 1-2 C + G2 Input C)*L.D.D G1 + I.D. G2

Wire 1-2 C = 2.0, G2 Input C=61fF

TABlh = TPhl G1 + (2.0 * 61fF) * TPhl G1 + TPlh G3

Cycle Time

Cycle Time = CLK-to-Q + Longest Delay Path + Setup + Clock Skew

Clock cycle must be \geq The Longest Path

Summary

- Die Equations
- Performance Equations
- Instruction Set Architecture:
 - Stack
 - Accumulator
 - General Purpose Register:
 - Register/Memory
 - Load/Store
- Addressing Modes:
 - Displacement
 - Immediate
 - Register Indirect
- Pipeline
 - Hazards:
 - Structural
 - Data
 - Control
- Internal Delay
- Clock Cycle