

Preview

I Little Endian versus Big Endian

Little 7 6 5 4 (Intel 80x86, Vax, ...)

Big 0 1 2 3 (HP-PA, MIPS, Motor..)

II Gate Technology

III 2's complement

IV Overflow/Underflow

V ALU

Administrative

- I Homework due by 2:30pm (no late)**
 - Individual Work**
- II Laboratory #1 due in next section**
 - Team of two persons**
- III Get to know people for Groups**
- IV Office hrs: Tue 6-7:30p, Thu 9:30-11a**

Computer Fun

- I Draw on a paper: Computer**
- II Update it every week**
- III By the end: complete computer**

Review

I Instruction Usage

A	Load	22%
B	Conditional Branch	20%
C	Compare	16%
D	Store	12%
E	Add	08%
F	And	06%
G	Sub	05%
H	Move Reg-Reg	04%
I	Others	06%

Review

I Data-types

II Data Addressing Modes

42% Average	- Displacement
33% Average	- Immediate
13% Average	- Register Indirect
12%	- Rest

Review

- I Computer Architecture**
= ISA + Organization
- II Five components of Computer**
- III Cost Equations**
- IV Execution Cycle: Pipeline**
- V Memory Hierarchy**

Review

- V ISA Classes**
 - A Accumulator**
 - B Stack**
 - C General Purpose Register**
 - D Load/Store**
 - E (Write pseudo code: $A=B+C-D$)**

- VI Instruction**
 - **Fixed length vs. Variable length**

CS 152

Discussion Section 102: Friday 12-2
Discussion Note #2: January 26, 1996

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Agenda

- I Review (20 min)**
- II Administrative/Break (5 min)**
- III Computer (5 min)**
- IV Discussion/HW (20 min)**
- V Group (5 min)**
- V Preview (20 min)**