Administrative

I Lab #5 due next week

- Group Work

II Roving T.A.s Schedules

III Design Review Today After Section

IV Get moving with Project

Preview

I Memory Hierarchy

Cache (SRAM)
Memory (DRAM)
Hard Disk
Tape

II Cache

Set-Associative
Direct Mapped

Review

II Microprogramming

Horizontal - More Control over Parallel
But it uses up lots of control store

Vertical - Easier to Program, like RISC
But extra level of decoding (slow)

Ease of Design, Flexibility, Powerful ISA
Generality, Compatibility, but Costly
and slow - Leads to RISC

Review

III Pipeline Hazards

Structural Hazard
Attempt to use same resource 2-way
Data Hazards
Instruction dependency
Control Hazards
Executing branch before cond

Solution: Waiting (Bubble) - Forward

Assignment 5 Questions

I Question

II Suggestions

Review

I Exceptions: Interrupts and Traps

Interrupts - Caused by External Events
- **Asynchronous to Program**
- **Maybe handled between instruction**
- **Simply suspend and resume user prg**

Traps -Caused by Internal Events(ovrfl..)
- **Synchronous to Prgram**
- **Conditions must be remedied (hndlr)**
- **Instr retried/Prog. Aborted**

CS 152

Discussion Section 102: Friday 12:30-2

Discussion Note #8: March 8, 1996

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Agenda

I Homwork Discussion (15 min)
II Review (10 min)
III Administrative/Break (5 min)
IV Preview (15 min)
V Multicycle-Processor (1 hour)