Administrative

I Cache Design due next week

- Group Work

II Design Review Today After Section

III Get moving with Project

IV Thinking about On-line turn-in

V Accounts: 1 big account 3 small accts

Preview

I More Memory

Cache

Set-Associative
Direct Mapped

II Memory

DRAM
SDRAM

Homework Questions

I Question

II Suggestions

Correction

I Alpha: DEC claims Alpha not GaAs

Layout done manually in transistor lvl?

Review

I Exceptions: Interrupts and Traps

II Microprogramming: H vs. V

Ease of Design, Flexibility, Powerful ISA
Generality, Compatibility, but Costly
and slow - Leads to RISC

III Pipeline Hazards

Structural Hazard
Data Hazards
Control Hazards

CS 152

Discussion Section 102: Friday 12:30-2

Discussion Note #9: March 15, 1996

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Agenda

I Homwork Discussion (15 min)
II Review (10 min)
III Administrative/Break (5 min)
IV Preview (15 min)
V Pipelined Datapath (1 hour)