DMA

I DMA - allows memory transfers w/o CPU

II Specific Functions

III More Genral Devices I/O Processors

LAN/WAN

I WAN: T1 - 1Mb/s, T3 - 45Mb/s

II LAN: Ethernet, Token Ring, Token Bus

LAN: FDDI, Myrinet

III Examples: GSC/Myrinet Card

Token Ring

Buses and I/O

III Bus Transactions

1. **Send Address**
2. **Send/Receive Data**

IV Design options

1. **Bus Width**
2. **Data Width**
3. **Transfer Size**
4. **Bus Master**

Buses and I/O

IV Design options

5. **Split Transaction**
6. **Clocking**

V Interrupt driven I/O

VI Interrupts allow CPU to run waiting

Cache

I Set Associativity

II Write-Through/Write-Back
Write-Allocate/Write-No allocate

III Advantages of using one from another

IV Trade-offs

V Blocks and Sets

Buses and I/O

I Two Major Advantages for BUS

1. **Low cost**
2. **Versatility**

II Types of Buses

1. **CPU-Memory Bus**
2. **I/O Bus**

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Hazards

I Pipeline Hazards

Structural Hazard

Attempt to use same resource 2-way

Data Hazards

Instruction dependency

Control Hazards

Executing branch before cond

Solution: Waiting (Bubble) - Forward

Memory Hierarchy

I Registers (SRAM or Latches)

II Caches (1st level and 2nd level) - SRAM

III Main Memory (DRAM)

IV Hard Disk

V Tape backup

Micropogram

I Microprogramming

Horizontal - More Control over Parallel
But it uses up lots of control store

Vertical - Easier to Program, like RISC
But extra level of decoding (slow)

Ease of Design, Flexibility, Powerful ISA Generality, Compatibility, but Costly and slow - Leads to RISC

Pipeline

I Laundry

II IF, ID, EX, MEM, WB

III Ideal 5 time speedup - hazard

IV Forwarding units

V Delay slots for Load and Branch

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Datapaths

I Single Cycle

II Multicycle

* Look in the book for logic design

* 307 for single, 323 for multicycle

** Lecture notes #9, #11

Exceptions and Traps

I Exceptions: Interrupts and Traps

Interrupts - Caused by External Events
- Asynchronous to Program
- Maybe handled between instruction
- Simply suspend and resume user prg

Traps -Caused by Internal Events(ovrfl..)
- Synchronous to Prgram
- Conditions must be remedied (hndlr)
- Instr retried/Prog. Aborted

Exceptions and stuff

I Exceptions: Interrupts and Traps

II Microprogramming: H vs. V

Ease of Design, Flexibility, Powerful ISA Generality, Compatibility, but Costly and slow - Leads to RISC

III Pipeline Hazards

Structural Hazard
Data Hazards
Control Hazards

Data

I Data-types

II Data Addressing Modes

42% Average - Displacement
33% Average - Immediate
13% Average - Register Indirect
12% - Rest

III Endian (Big vs. Little)

Single Cycle Datapath

Comment: Very important to know.

I Datapath - What CS152 is all about

II Draw your idea of Computer

III Block Diagram

IV Study Lecture notes

V Control & HDL

Floating Point Number

Comment: Important - Standardized in the World

I IEEE standard - Professor Kahan

II Floating Point Add and Multiply

III S:1-sign, 8-exp, 23-significand
D:1-sign, 11-exp, 52-significand

Equation:
-1*sign*(1.significand)*2^(exp-127)

ALU

Comment: Should know from Lab 3

I Problem 4.4 in Quiz #1

II Ripple carry?!?

III Carry Look Ahead

IV Carry Select

V Combination!!!

Arithmetic

Comment: Computer Arithmetics, Symbolic

I 2's Compliment Number

II Addition and Subtraction

III Multiply

- Implementation? (Algorithm)

- Final design in the book (Hardware)

- Booths Method

Technology

I NMOS - no bubble, conducts when gate is high

PMOS - bubble, conducts when gate is low

*** If PMOS is faster NOR**

*** If NMOS is faster NAND**

IV Cycle time = CLK-to-Q + Longest Delay path + Clock Skew

Hold Time < CLK-to-Q + Shortest Delay path - Clock Skew

Technology

Comment: Real issue in hardware implementations

I CMOS technology

- Lecture notes #5

II Internal Delay - LDD

III Cycle time

IV Problem 4.3 in Quiz #1

SPARC STATION

I **Datapath + Control (CPU)**

II **CPU + Coprocessors**

III **Memory + Controller**

IV **BUS**

V **I/O: Hard Disk, Floppy, Keyboard**

Classes

V **ISA Classes**

- **A** **Accumulator**
- **B** **Stack**
- **C** **General Purpose Register**
- **D** **Load/Store**
- **E** **(Write pseudo code: A=B+C-D)**

VI **Instruction**

- **Fixed length vs. Variable length**

ISA

Comment: Important to be familiar with MIPS because you will be implementing it in your design

I Questions to examine from Quiz #1

- Problem 3.3 and 3.5

II There are problem in sections 3.9 and 3.10 in book

III Look back homework #2

MIPS Assembly Language

I Crucial to know MIPS Assembly

II Laboratory #2

III Read Appendix + Recommended book

IV Swap code

```
lw $15, 0($2)        # load v[0] to reg15
lw $16, 4($2)        # load v[4] to reg16
sw $16, 0($2)        # store old v[0]->v[4]
sw $15, 4($2)        # store old v[4]->v[0]
```

Amdahl's Law

Speedup due to Enhancement

$$= \frac{\textbf{Execution time without Enhancement}}{\textbf{Execution time with Enhancement}}$$

Equation:

ExecutionTimeW/Enhance = ExecTimeWithoutEnhance*(F/S+(1-F))

Instruction Set Architecture

I VAX (CISC)

- **A Variable Length Instructions**
- **B Many, many, many instr. types**

II MIPS (RISC)

- **A Fixed length**
- **B About 50-80 Instructions (How?)**
- **C Simple Instructions**

Cost

Comment: Important for profit reasons

I Equations - Die Equations (Compiled in Notes)

II Look into question from Quiz #1

- Problem 2.11

Processor Metrics

Equations:

Execution time = Clock Cycles/Program * Clock Cycle time

Execution time = Clock Cycles/Program/Clock Rate

Clock Cycles/Program = Instr./Program * CPI

CPI = Clock Cycles/Program/(Instr./Program)

CPI = (CPU Time * Clock Rate)/Instruction Count

Performance

Comment: Important to keep this in mind when evaluating computers

I Speedup - Amdahl's Law (Concept in Quiz #1)

II Compiler Problem - MIPS and CPI

III Equations (In Lecture notes)

IV Frequently missed problems in Quiz - Problem 2.5 (Solution set) and 2.9

COST

Equations:

```
                         Wafer Cost
Die Cost = ----------------------------
             Dies per Wafer * Die Yield

                               Wafer Yield
Die Yield =-----------------------------------------
           (1+(Defects per unit area * Die Area)/a)^a

               pi*(Wafer D/2)2   pi*Wafer D
Dies/Wafer = --------------- - ----------- - Testdies
                die area      sqrt(2*DieArea)
```

CS152

I Whot's Compoota?

- **A Brief History - ENIAC, EDSAC, ...**
- **B CISC versus RISC**
- **C Future MPP, NOW**

II Structure

- **A Pipeline**
- **B ISA + Organization**
- **C Microprocessor Performance (Yikes!)**

Common Sense: 5 Basic Comp

I Datapath

II Control

III Memory

IV Input

V Output

Final Outline

XV Cache

XVI Virtual Memory

XVII BUS - PCI

XVIII Input and Output

XIX LAN/WAN

What, When, and Where

I What: May bring one 8.5 x 11 cheat sheet, front and back.

II When: This Friday, May 10
8AM - 11AM

III Where: Etcheverry 3106
Exam group #1

Final Outline

I Organization Performance/Cost

II Instruction Set Architecture

III Technology

IV Arithmetic Logic Unit

V Numberic System - Arithmetic

VI Multipliers - Algorithm

VII Divide and Floating point

Final Outline

VIII Single Cycle Datapath

IX Multicycle Datapath

X Interrupts and Exceptions

XI Microprogramming

XII Pipelining

XIII Hazard

XIV Memory Hierarchy

CS 152

Final Review

Discussion Note #1: May 7, 1996

6-8pm @ 306 Soda

E-mail: youngc@cs.berkeley.edu
Homepage: http://http.cs.berkeley.edu/~youngc
Office: 466 Soda Hall Phone: 642-9076

Agenda

I Outline

II What, When, & Where

III Problems

IV Questions