University of California, Berkeley
Computer Science and Electrical Engineering
Computer Science 152
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Discussion section 102

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Class Diagnostic Quiz: Solution

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Write the answers to STARed questions on a separate piece of paper.

Common sense questions:

*1.1 Name five classic components of computer.
Read Page 16

1. Control
2. Datapath
3. Memory
4. Input
5. Output

1.2 What is the rate of capacity change for DRAM (often called DRAM rule of thumb)?
Read Page 22

Four times every 3 years

1.3 What's the name of the first electronic computer with 18,000 vacuum tubes with 20-10 digit registers.
Read Pages 31-33

ENIAC: First general-purpose electronic computer operational during WW II, 1947
EDSAC: First Full-scale stored program computer 1949

Performance questions:

2.1 What is a relation between Performance and Execution time?
Read Page 50

$$\text{Performance} = \frac{1}{\text{Execution Time}}$$

2.2 What is the most accurate representation computer performance?
Read Pages 52-53

Time

2.3 If machine A runs a program in 25 seconds and machine B runs the same program in 40, how much faster is A than B?
Read Example in Page 51

40/25 = 1.6 times
A is 1.6 times faster than B

2.4 What is the equations for CPU execution time for a program using variables (a) Instruction count, CPI, Clock rate, and (b) Instruction count, MIPS?
Read Pages 57, 61

*2.5 Consider the machine with three instruction classes and CPI

Instruction Class	Class A - 1 cycles	Class B - 2 cycles	Class C - 3 cycles
I-count from Cmpiler Y	5 million	2 million	1 million
I-count from Cmpiler Z	20 million	1 million	1 million

Machine runs 150Mhz. Calculate MIPS and CPU time for instruction output from both compilers Y and Z. What does this tell you about MIPS?
Read Example in Pages 61-63

CPI_1 = $((5*1+2*2+1*3)*10^6) / ((5+2+1)*10^6) = 12/8 = 1.5$
$MIPS_1$ = Clock Rate / ($CPI*10^6$) = 150 Mhz/1.5 = 100 MIPS
CPU $Time_1$ = Instruction per Program / MIPS = (5+2+1)/100 = 0.08 sec

CPI_2 = $((20*1+1*2+1*3)*10^6) / ((20+1+1)*10^6) = 25/22 = 1.136$
$MIPS_2$ = Clock Rate / ($CPI*10^6$) = 150 Mhz/1.136 = 132 MIPS
CPU $Time_2$ = Instruction per Program / MIPS = (20+1+1)/132 = 0.167 sec

This tells you MIPS reading sucks (Just Kidding). Higher MIPS does not necessarily mean better performance.

2.6 Write an equation for MFLOPS.
Read equation on Page 64

2.7 Write an equation for geometric mean and harmonic mean. Briefly explain why these are better than arithmetic mean.
Read the equations in Pages 75, 87

2.8 What is the general idea behind Amdahl's law?
Read Page 89

*2.9 Consider the problem of going from Nevada to California over Sierra Nevada mountains and through desert to LA. Your walk over the mountains will take 20hours. The last 200 miles, however can be done by high-speed vehicle. There are three ways to complete your journey.
(a) continue walking at average of 4 miles/hour.
(b) drive awesome Korean-made Hyundai Excel at average of 50 miles/hour.
(c) fly on Southwest at average of 600 miles/hour.
What are the speedups for different vehicles for the entire trip?
Read Page 89

Time = Exec Time unaffected + Exec Time effected/Rate of improvement
Speedup = Execution time before improvement/Execution time after improvement
(a) Time = 20 + 200/4 = 70 hours, Speedup = 1
(b) Time = 20 + 200/50 = 24 hours, Speedup = 2.91
(c) Time = 20 + 200/600 = 20.34 hours, Speedup = 3.44

2.10 Write equation for die yield.
Read Page 44

*2.11 Given wafer yield is 90%, alpha for simple MOS=2.0, defects per unit area=2 square cm, and die area is 1 square centimeter, what is the die yield?
Read Page 44, discussion note #2 or lecture notes

$$\text{Die yield} = \frac{\text{wafer yield}}{(1+(\text{defect per area} * \text{die area})/\text{alpha})^{\text{alpha}}}$$

= 22.5 %

Instruction Set Design:

*3.1 What would C compiler produce in MIPS architecture for following line?
f = (a + b) - (c * d);
Read Pages 97-98, 111, 136-137, 138-142*

go over the examples in the book, since this is too simple example.

*3.2 What would be a faster way to multiply value of register $8 by 16 than using add-shift multiply algorithm or multiply instruction? (hint: use just one simple MIPS instruction)
Read Appendix A

```
sla $8, $8, 4                    ;shift left arithmetic 4 time
```

*3.3 Draw three different formats of instruction in MIPS ISA and name them.
Read Page 291

R-type instruction

Opcode	rs	rt	rd	shamt	funct
31 26	25 21	20 16	15 11	10 6	5 0

Load or Store instruction

35 or 43	rs	rt	address
31 26	25 21	20 16	15 0

Branch instruction

4	rs	rt	address
31 26	25 21	20 16	15 0

3.4 What is the most frequently used addressing mode?
Read lecture note

Displacement mode by 43%

*3.5 Write pseudo assembly codes for (a)accumulator architecture, (b)stack architecture, and (c)load-store general purpose register architecture for the following code.
a=(b + c) + (d - c);
Read lecture notes

(a)		(b)		(c)	
load	AddrB	push	AddrB	load	$1, AddrB
add	AddrC	push	AddrC	load	$2, AddrC
save	AddrT	add		load	$3, AddrD
load	AddrD	push	AddrD	load	$4, AddrC
sub	AddrC	push	AddrC	add	$5, $1, $2
add	AddrT	sub		sub	$6, $3, $4
save	AddrA	add		add	$Result, $5, $6
		pop	AddrA		

Technology:

4.1 If PMOS was faster which kind of gate would be best?
Read Lecture Notes

NOR

4.2 When a HIGH is applied to PMOS transistor, what happens to the gate for the conduction path?
Read Lecture Notes

gate is closed. No current flows through. "Shuts off conduction path"

*4.3 Other than internal delays of the gates of the critical path, what other thing(s) must be considered for the cycle time?
Read Lecture notes

1. gate input capacitance
2. load dependent delay
3. wire capacitance
4. clock skew
5. setup+holdtime (usually ok since a lot of gates)

*4.4 Draw a full-adder using gates.
Read cs150 book... This word processor is too good with graphics

Sum = (A xor B) xor C_{in}
C_{out} = (A or B) or (C_{in} or A) or (C_{in} or B)