CS152 Diagnostic Quiz Part 1

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Microprogramming:

*1. Do Exercise 5.16 from the textbook.

Pipelining/Hazards:

*2. Assume that a, b, c, d, e, and f are in memory. Write code for the pipelined MIPS corresponding to the following high-level code:

```
a = b + c;
d = e - f;
```

Your code should have as few stalls as possible, i.e., switch the order of instructions if it helps. Assume that all forwarding logic is present, and that loads and branches have one delay slot.

Memory System:

*3. Here is a table containing cache miss rates for different cache sizes and types:

Size	Instruction Cache	Data Cache	Unified Cache
16K	0.64%	6.47%	2.87%
32K	0.39%	4.82%	1.99%

You have a choice of two different cache setups for your machine:

A. A 16K instruction cache and 16K data cache.
B. A 32K unified cache (instruction and data are in the same cache).

Assume that 75% of all memory references are instruction references while 25% are data references. A cache hit takes 1 clock cycle and the miss penalty is 10 clock cycles for all the caches. Also, for a unified cache, a hit on a load or store instruction takes 2 clock cycles instead of 1 because there is only one cache port to satisfy two simultaneous requests. What are the miss rates for each of the setups A and B? What are the average memory access times for A and B?

*4. Given figure 5.5 (from the textbook) write out the microcode sequence for memory references, branches, and jumps (i.e., for R-type instructions):

Label	ALU Control	Src1	Src2	ALU Dest	Mem	MemToReg	PC Write	Seq
Rformat1	Func code	rs	rt					seq
	Func code	rs	rt	rd				fetch

5. Name the different kinds of buses and their functions.

*6. What are the steps in the asynchronous handshaking protocol to read a word from memory and receive it in an I/O device?

*7. Draw out the multicycle datapath?

8. Consider an unpipelined machine with five execution steps of latencies 50ns, 50ns, 60ns, 50ns, 50ns. Suppose that due to clock skew and setup time, pipelining the machine adds 5ns of overhead to each execution step. How much speedup in the instruction execution rate will be gained from pipelining?

9. How many total bits are required for a cache with 128K of data?

10. There are two very similar computers with the same cache performance. The instruction cache miss rate for program 1 is 3% and the data cache miss rate is 15%. Computer A has a CPI of 3 without any memory stalls and computer B has a CPI of 4 without any memory stalls. Assume that the miss penalty for both computers is 15 cycles. What is the performance ratio? (Give the answer in terms of which computer is faster and by how much.) Assume that both computers have the same clock cycle time.

11. Given that the instruction count is 2.5 million, computer A has a clock rate of 50Mhz, and computer B has a clock rate of 66 Mhz, what are the CPU times for program 1 in both computers? What is the performance ratio now?

12. Define a direct-mapped cache in terms of an n-way set associative cache.

13. Which of the following instructions will cause a data hazard?

```
ADD R1, R2, R3
SUB R4, R1, R5
AND R6, R1, R7
OR R8, R1, R9
XOR R10, R1, R11
AND R8, R1, R2
SUB R10, R1, R2
ADD R1, R2, R3
LW R4, 0(R1)
SW R1, 12(R1)
SW R4, 20(R4)
```

14. There are three types of hazards:

RAW (Read After Write)
WAR (Write After Read)
WAW (Write After Write)

Classify each of the hazards you found in question 13 as one of the above three types.

15. For the instructions above, put in the minimum number of nop instructions to remove all hazards.

16. Define write-through and write-back caches.

17. What are write-allocate and no write-allocate caches? Which of these two is typically implemented on a write-through cache? Which of these is typically implemented with a write-back cache? Why?