CS152
Laboratory #4: Design Review
Discussion 102: Friday 12:30-2:00pm
Review Date: February 28, 1996
Due Date: March 1, 1996

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Group Name: _____
Group Account: _____
Total Points: _____

I Introduction.....(/10)
- A Cover sheet.....(/01)
- B Table of Content.....(/01)
- C Background.....(/08)

II Laboratory Exercises.....(/70)
- A Step 0: Building VHDL model.....(/04)
  - 1 buft32.vhd
  - 2 Symbol
- B Step 1: VHDL Implementation.....(/12)
  - 1 Brief description
  - 2 Component testing
  - 3 Encapsulation of adder - CP
  - 4 ALU encapsulation
  - 5 Comparator in gates and VHDL
  - 6 Extender in VHDL
- C Step 2: Single Cycle Datapath.....(/20)
  - 1 Initial datapath (step 2.1)
  - 2 Decoder (step 2.2)
- D Step 3: PC and Memory.....(/20)
  - 1 PC in VHDL
  - 2 Datapath with PC and Memory
  - 3 Testing Procedures
  - 4 lw and sw implementation
  - 5 jr and beq implementation
- E Complete Single Cycle Datapath.....(/14)
  - 1 Show that datapath complete and functional

III Conclusion.....(/10)
- A Results
- B Experience - Partnership
- C Future

IV Appendix.....(/10)
- A Other Testing Vectors
  - 1 On all the components in Step 0 and 1
  - 2 Progressive testing vectors for Single Cycle Datapath
- B VHDL code listings
- C Logs and others