

Personal Portfolio

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Contact Information

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Education

Masters in Computer Engineering
University of Texas at Austin
Anticipated on December of 2000

Bachelors in Computer Science
University of California at Berkeley
Received on May of 1996

Recent Projects

01.	M2L-M2SC v.2.2	Jul 99	Myrinet (LAN/SAN) to Fiber - IDT FIFO modification
02.	M2L-M2SC v.2.1	Apr 99	Myrinet (LAN/SAN) to Fiber (High Availability + 10km)
03.	M2L-M2SC v.2.0	Feb 99	Myrinet (LAN) to Fiber (old chipset + 2km)
04.	M2L-M2SC v.1.0	Jun 98	FI/Fiber test board - board design/FPGA/test software (2km)
04.	L4.X Logic Analyzer	May 98	LANai 4.X based logic Analyzer
05.	Quad LANai 5.0	Feb 98	Scalable two-level computing unit LANai 5.0 processor + 8 port switch
06.	M2M-OCT-SW8 v1	Sep 97	Myrinet 32 port switch board design
07.	Channel Router v0.98	Aug 97	Board routing CAD tool for Myrinet board design
08.	Sandia ATR System	Jun 97	Implementation of ATR system on scalable two-level multicomputer
09.	Dual SAN/LAN board	Jun 97	Two channel SAN to LAN/LAN to SAN conversion board
10.	BGA Switch Test board	May 97	Test board for new BGA packaged 8-port Switch chip
11.	LANai 4.x Multicomputer	Feb 97	Research/development of scalable general two-level computing
12.	L4.x Test Board	Dec 96	Test board modified & re-configured for LANai 4.x chip
13.	L5.x Test Board	Nov 96	Design universal chip test board & FPGA (used for LANai 5.x/6.x)
14.	FI Test System	Sep 96	Test hard/software development for Myrinet fiber interface chip
15.	FPGA Ctrl CAD	Aug 96	CAD software for internal hardware/FPGA code development
16.	Hand-Shape Recognition	May 96	Virtual Reality Hand Shape Recognition via ordinary Camera
17.	VLIW processor	May 96	VLIW RISC processor transistor level simulation
18.	GSC+/Myrinet board	May 96	LANai 4.x based Network Interface Board for HP GSC+ Bus

Employments

1.	Aug 99 -Present:	University of Texas, Austin, Applied Research Laboratories Graduate Research Assitant
2.	Jul 96 - Aug 99:	Myricom, Inc. (Leave of Absence) Engineer/Researcher
3.	May 95 - Jul 96:	Department of Computer Science, UC Berkeley Senior Engineering Aid - NOW Project - CAL group
4.	Dec 95 - May 96:	Department of Computer Science, UC Berkeley Student Instructor for Upper Division CS Architecture

Award

Certificate for Outstanding Achievements
Student Instructor for CS152 - UC Berkeley Upper Division CS Architecture Course

Skills

1. PC Board design/CAD tool
PCB: PADS, Powerview, Workview, Xact, Route/Channel/XPE (internally developed CAD)
Logic: Epic, Cosmos, Verilog, Powerview, PADS, MAX Plus II, XPE/FPGA_ROM (internal)
FPGA: Xilinx, Altera, ORCA
Chip Layout: Cadence, Synergy
2. Computer System Development
Compilers: lanai3_gcc, GNU C/C++, Visual C++, Pascal, Visual Basic, COBOL
Scripts: Perl, Java, CLisp/Scheme, HTML
Logic Design Language: VHDL, Verilog, AHDL
Assembly language: LANai 4.1, VAX, MIPS
3. Network
Protocol: Myrinet Control Protocol, Message Passing, TCP/IP, UDP, Slip/PPP
Physical: Myrinet (SAN/LAN/Fiber), G-link interface, Fibre Channel, Gigabit Ethernet
4. Computer Platforms
Hardware: UC Berkeley NOW, Myricom Two-level Multicomputer, SPARC, Macintosh, PowerPC, x86
O/S: SunOS/Solaris, Windows 9x/NT, Linux, HP-UX, Mac OS, DOS

Others

1. GRE Computer Architecture session lecturer (CS re-entry program)
2. Computer Science Tutor in Berkeley CS Department (Comp. Sci. 150, 152)
3. Computer Science Teacher in High school level
4. Office/Computer manager for Valley Catholic Church (2 years)
5. Sunday School Teacher (4 years)
6. Church Choir Tenor (6 years)
7. Public Library volunteer (4 years)
8. Chamber of Commerce at City of Chatsworth, Ca (2 years)
9. Private Tutor (8 years)

References

1. Professor Brian Evans
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2. Charles Seitz, Ph.D.
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